REMARKS

In the Office Action mailed on June 28, 2005, Claim 21 is objected to because of an informality, and has been amended to refer to "integrated circuit die" in place of "integrated circuit" in lines 6 and 7. Claims 1-7, and 32 are rejected under 35 USC §102(b) as being anticipated by Seefeldt et al. (U.S. Patent 4,978,633, "Seefeldt"). Claims 21-25 and 30-31 are rejected under 35 USC §102(b) as being anticipated by Shimizu et al. (U.S. Patent 5,341,049, "Shimizu"). Claims 26-29 are rejected under 35 USC §103(a) as being anticipated by Seefeldt.

Response to Rejection of Claims under 35 USC §102(b) over Seefeldt

In response to the rejection of claims 1-7 and 32 under 35 USC §102(b) as being anticipated by Seefeldt, Applicant respectfully requests reconsideration of the rejection of claims 1-7, but has amended claim 32 to overcome the rejection. Regarding independent claim 1, it is suggested in the Office Action that the first plurality of regions is disclosed by gate supercells 31 and input/output supercells 32, and that the second plurality of areas comprises the 6 columns of a 6x6 array of Seefeldt. It is further suggested that each area of the second plurality comprises predetermined regions of the first plurality because each column has supercells 31 and 32. However, the only designation of regions of an IC in Seefeldt is the designation of either I/O supercells or gate supercells. A region defined as a combination of an I/O supercell and a gate supercell is inconsistent with the disclosure of Seefeldt. That is, Seefeldt teaches away from combining I/O supercells and gate supercells by defining these supercells separately. Because a region of Seefeldt does not include both I/O supercells and gate supercells, Seefeldt fails to disclose or suggest an IC having regions and areas wherein "each of the predetermined regions in a first area comprises programmable circuits which are substantially identical and have a first function and each of the predetermined regions in a second area comprises programmable circuits which are substantially identical and have a second function." That is, if the "second plurality of areas" is defined by the columns of a 6x6 array of Seefeldt, there is not teaching or suggestion that (i) each of the

predetermined regions in a first area (i.e. first column) has a first function and (ii) each of the predetermined regions in a second area (i.e. second column) have a second function as claimed. Accordingly, Applicant respectfully requests reconsideration of the rejection of claim 1 and dependent claims 2-4.

Similarly, referring to independent claim 5, Applicant respectfully submits that the elements of Seefeldt cited in the Office Action do not disclose the elements of Applicant's claims. It is suggested in the Office Action that the first set of regions of claim 5 is disclosed by "regions having I/O and gate" supercells of Seefeldt. It is also suggested that each region of the first column consisting "essentially of regions from the first set" is disclosed by the left-most column in Fig. 2 having I/O supercells and gate supercells. However, as set forth above, there is no teaching or suggestion that I/O and gate supercells in a column are grouped in a region. That is, the only regions defined in Seefeldt are the separate I/O regions and gate regions. Accordingly, each region of the first column Seefeldt does not consist essentially of regions from the first set (i.e. regions having an Input/Output circuit) as set forth in claim 5. It is also suggested that the second column of the third set is disclosed by the column next to the left-most column and consists essentially of gate supercells, and that the second column is disposed between the left-most column (i.e. the nearest side edge of the die) and the right column. However, the right column is also not a column of the first set for the same reasons that the left-most column is not a column of the first set. That is, there is no right column consisting essentially of regions of the first set. Applicant respectfully requests reconsideration of claim 5 and dependent claims 6-7.

In response to the rejection of claim 32 as being anticipated by Seefeldt, Applicant has amended claim 32 to include "a plurality of tiles in a second column extending from a first end to a second end, wherein the plurality of tiles comprises memory cells." Applicant respectfully submits that Seefeldt fails to disclose or suggest an integrated circuit comprising a column of memory cells, and respectfully requests reconsideration of claim 32 in view of the amendment.

Response to Rejection of Claims under 35 USC §102(b) over Shimizu

In response to the rejection of claims 21-25 and 30-31 under 35 USC §102(b)

as being anticipated by Shimizu, Applicant has amended independent claims 21 and 30 to overcome the rejection. In particular, Applicant has amended independent claim 21 to indicate that the plurality of configurable logic blocks in the first column have the same function, and has added a step of "providing a plurality of tiles in a third column extending from the first side of the integrated circuit die to the second side of the integrated circuit die, the plurality of tiles in the third column having different functions than the function of the first column." Applicant respectfully submits that Shimizu does not disclose or suggest both a first column of configurable logic blocks having the same function and another column of configurable logic blocks having different functions than the configurable logic blocks of the first column. Applicant respectfully requests reconsideration of the rejection of claim 21 and dependent claims 22-25.

Finally, Applicant has amended independent claim 30 to recite "a plurality of tiles disposed in a column on an end of the integrated circuit, wherein the plurality of tiles comprises a plurality of transceivers." Applicant respectfully submits that Shimizu does not disclose or suggest a plurality of transceivers disposed on an end of the integrated circuit. Applicant respectfully requests reconsideration of the rejection of claim 30 and dependent claim 31.

Response to Rejection of Claims under 35 USC §103(a) over Seefeldt

In response to the rejection of claims 26-29 under 35 USC §103(a) as being unpatentable over Seefeldt, Applicant has also amended independent claim 26 to include "a second column of input/output block tiles disposed on an end of the integrated circuit." Applicant respectfully submits that Seefeldt does not disclose or suggest both a first column of input/output block tiles, and a second column of input /output block tiles disposed on an end of the integrated circuit. Applicant respectfully requests reconsideration of the rejection of claim 21 and dependent claims 27-29.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 28, 2005.

Pat Slaback
Name

Signature